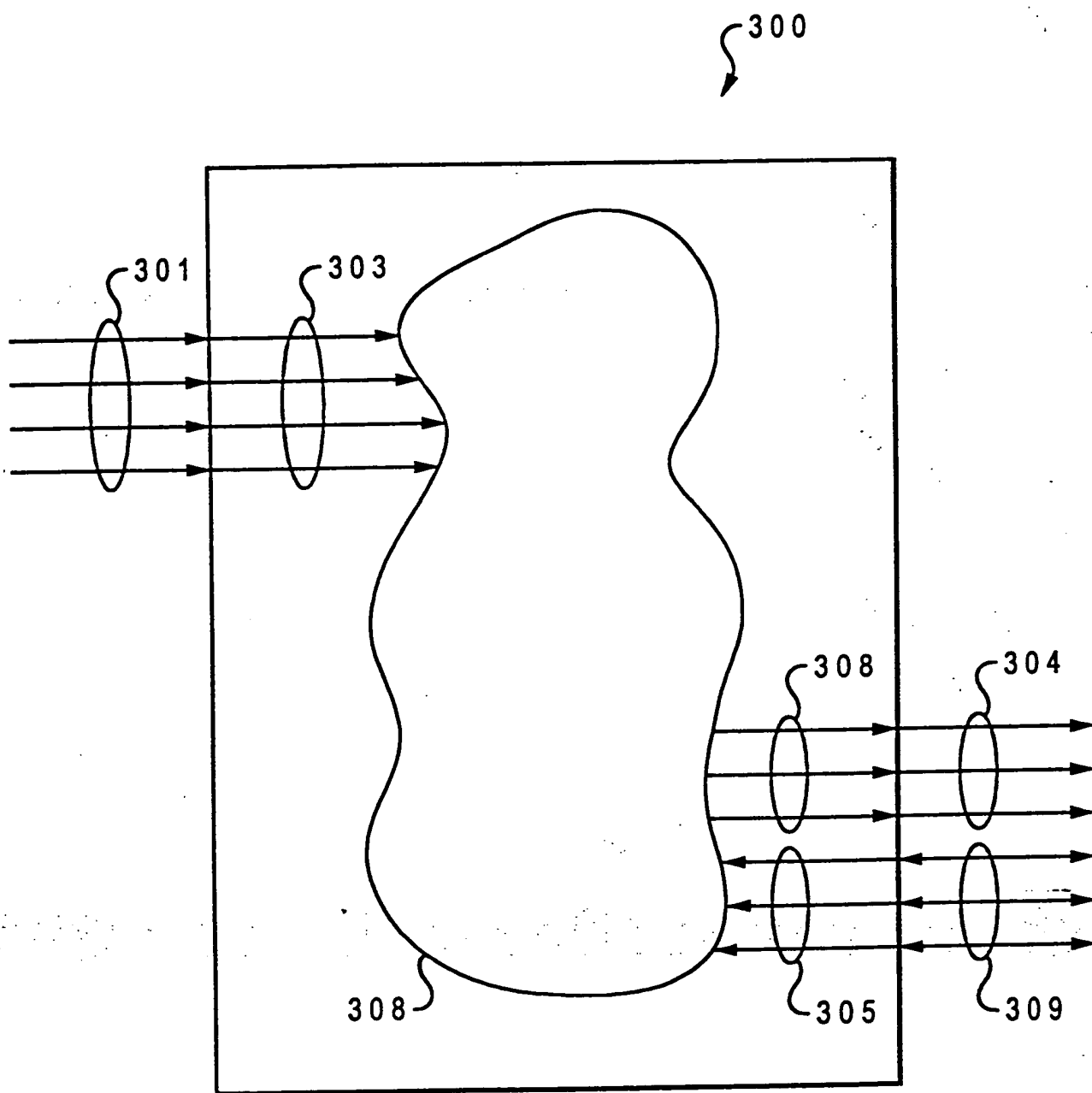


*Fig. 2*



*Fig. 3A*

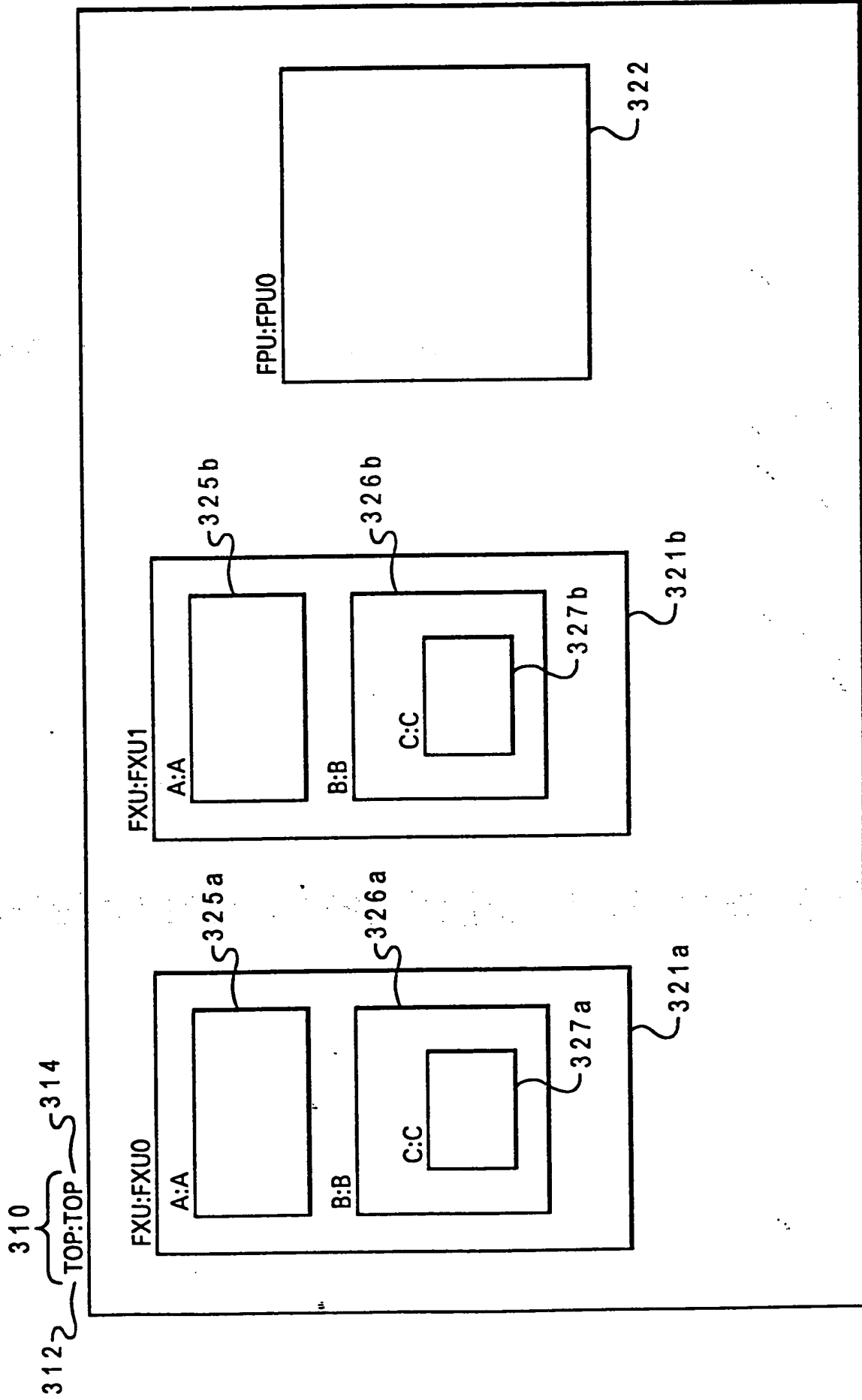


Fig. 3B





iii

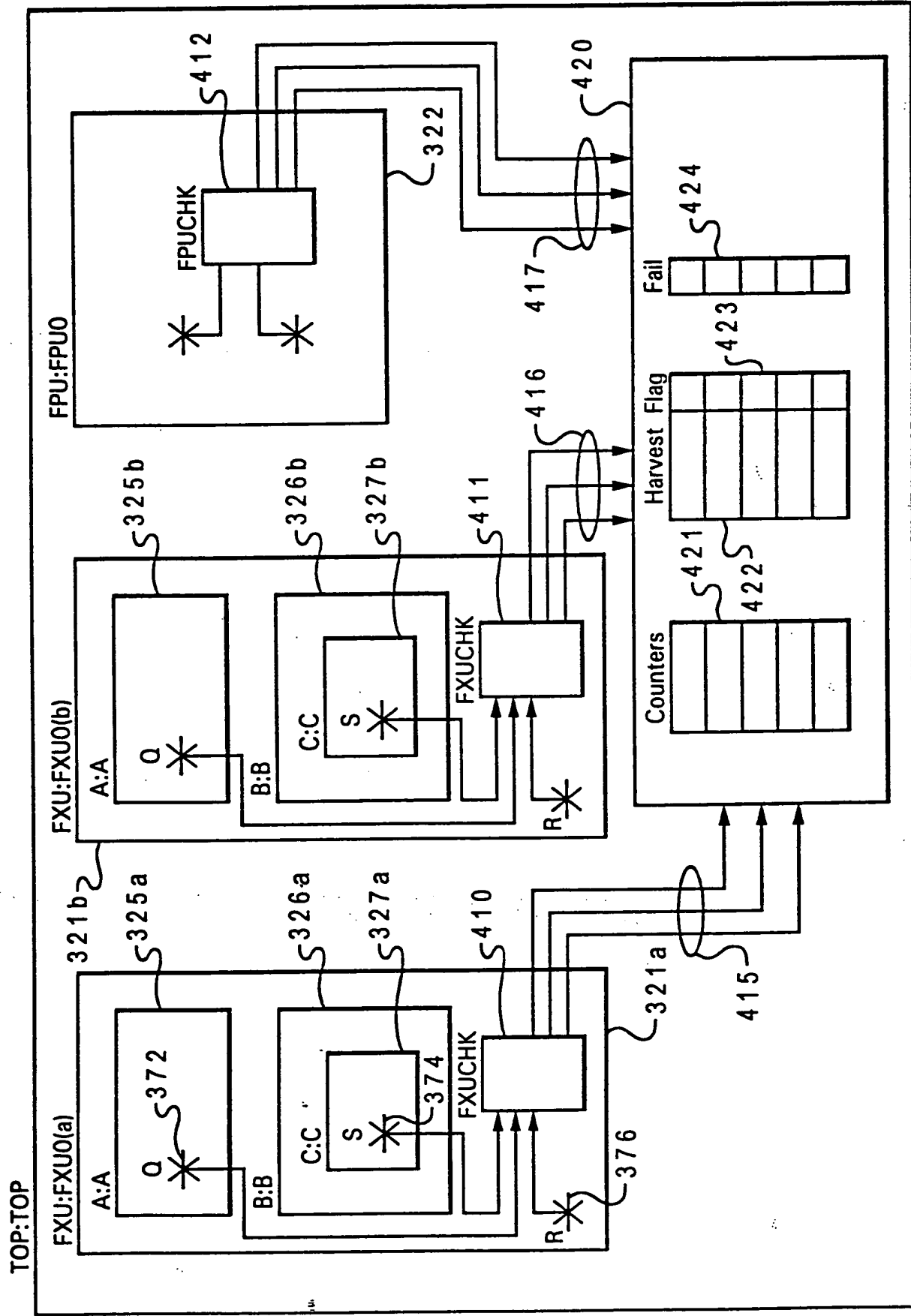


Fig. 4B

# THEORY

*Fig. 4C*

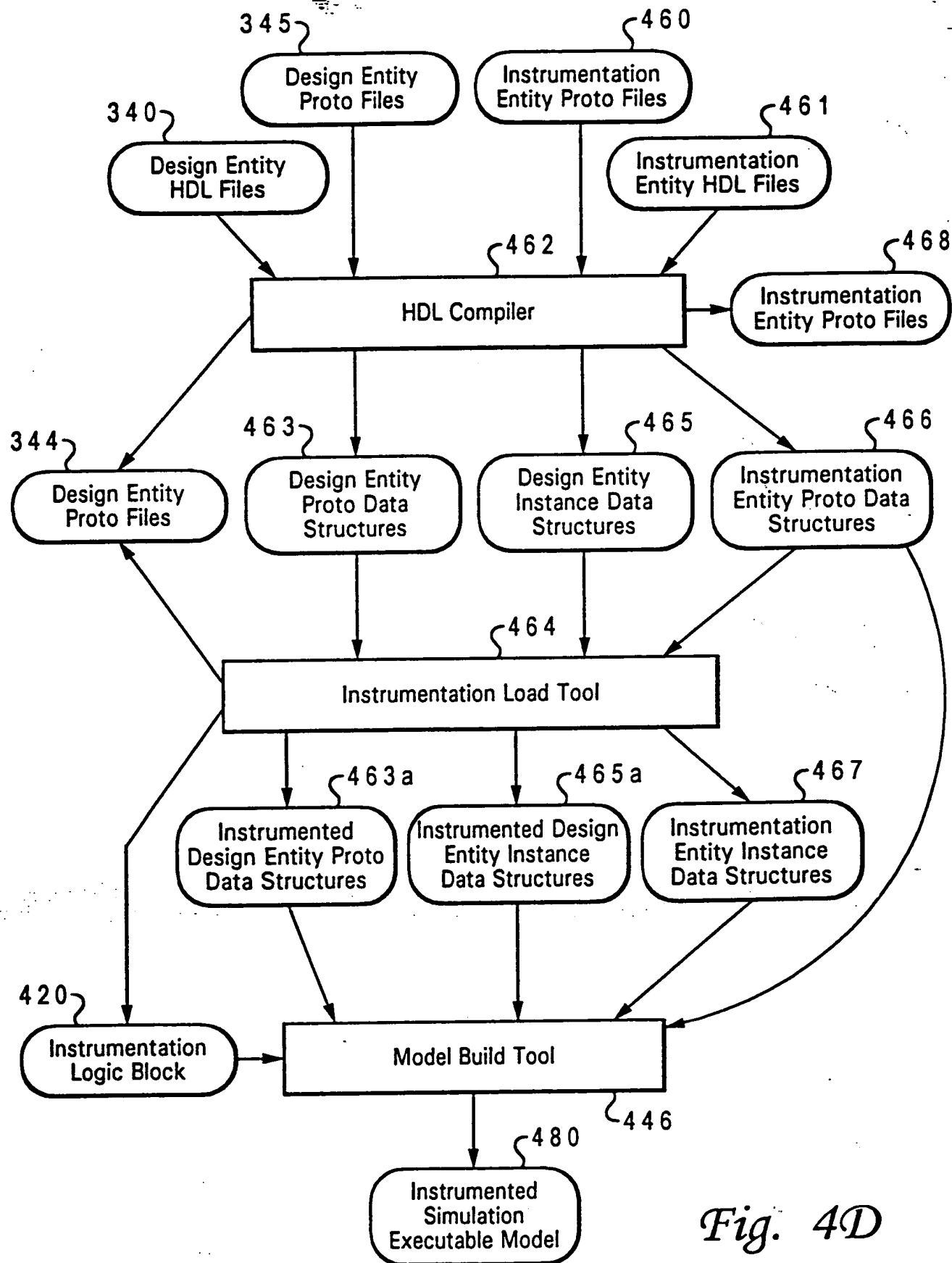


Fig. 4D

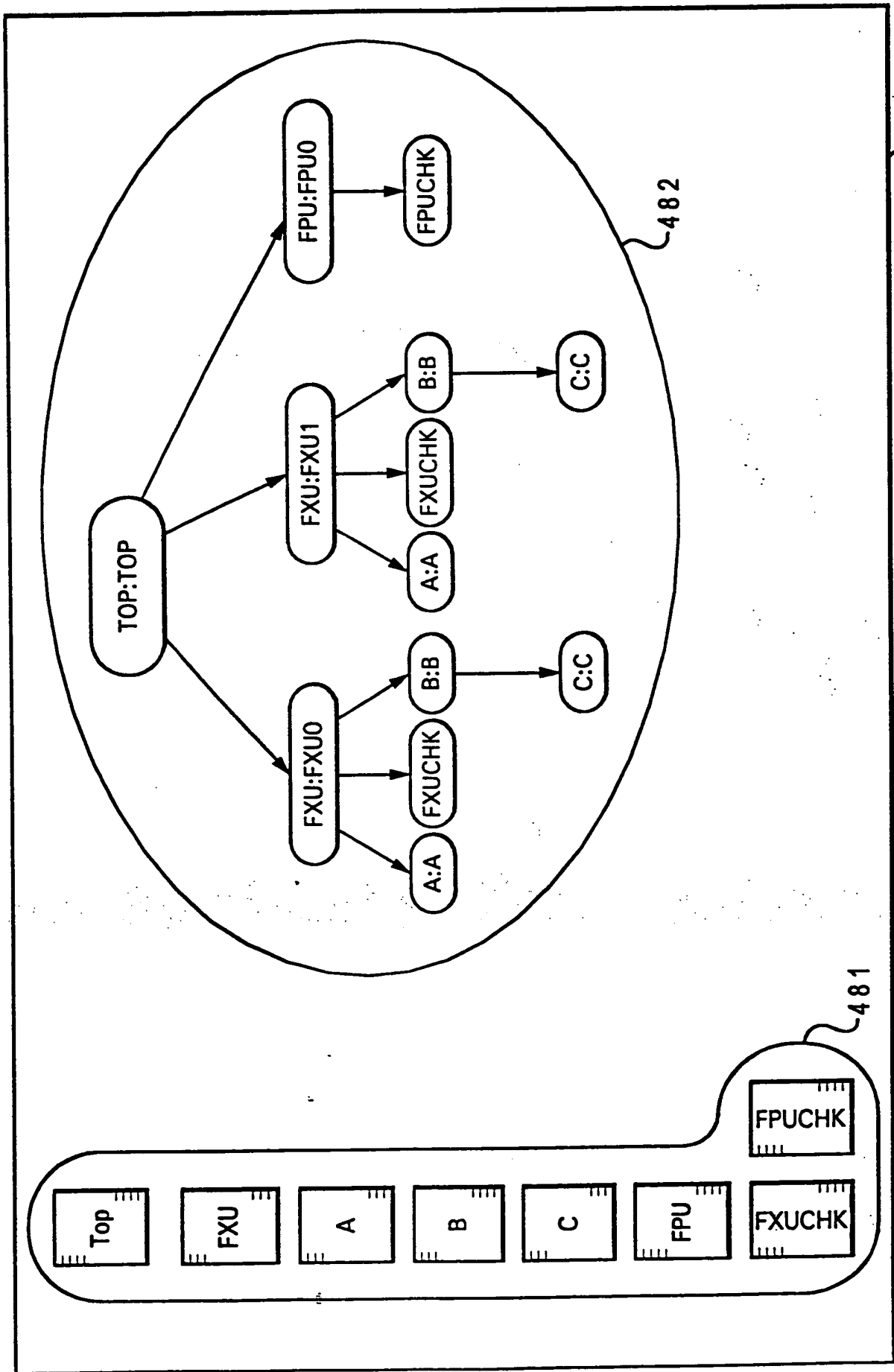


Fig. 4E

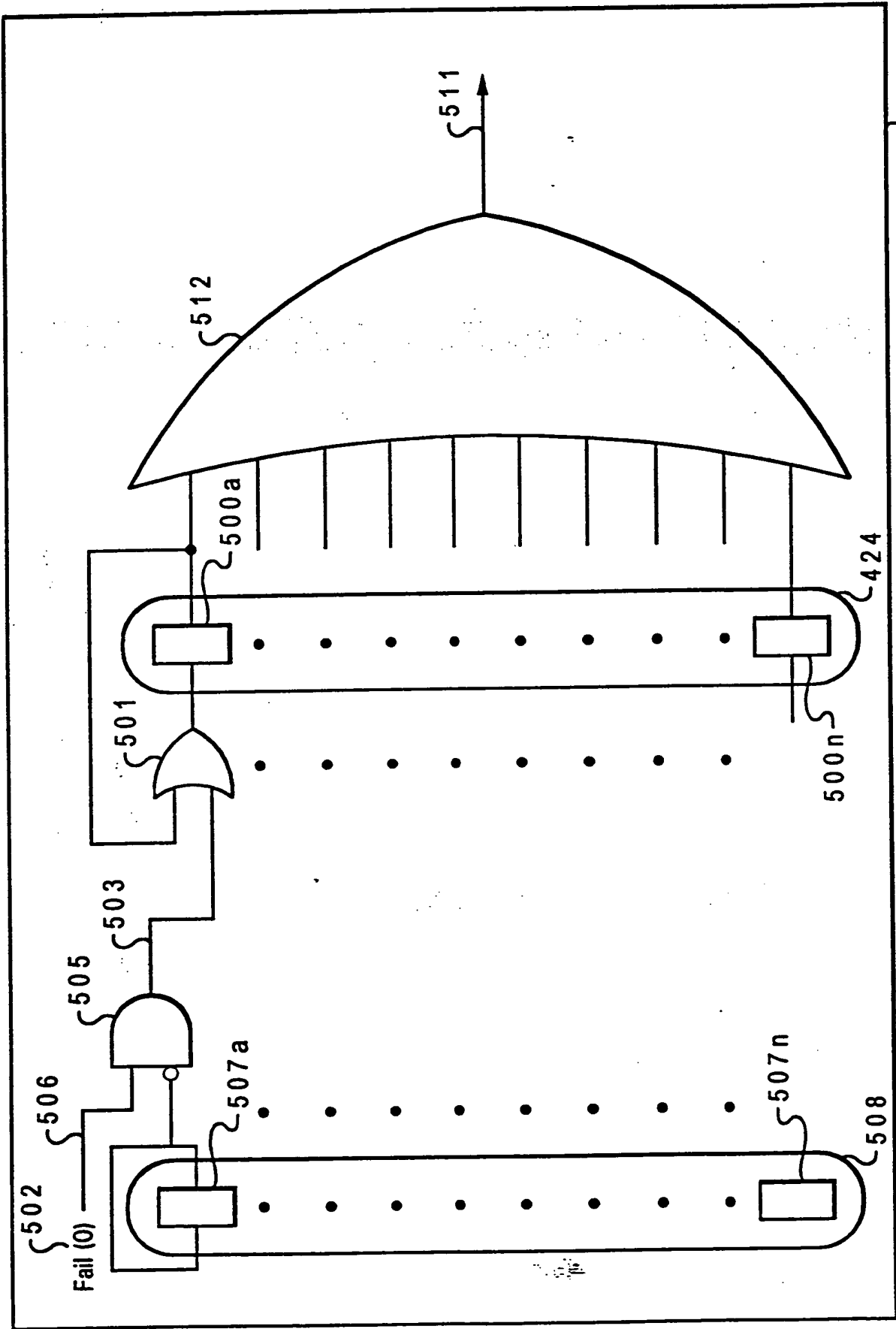


Fig. 5A

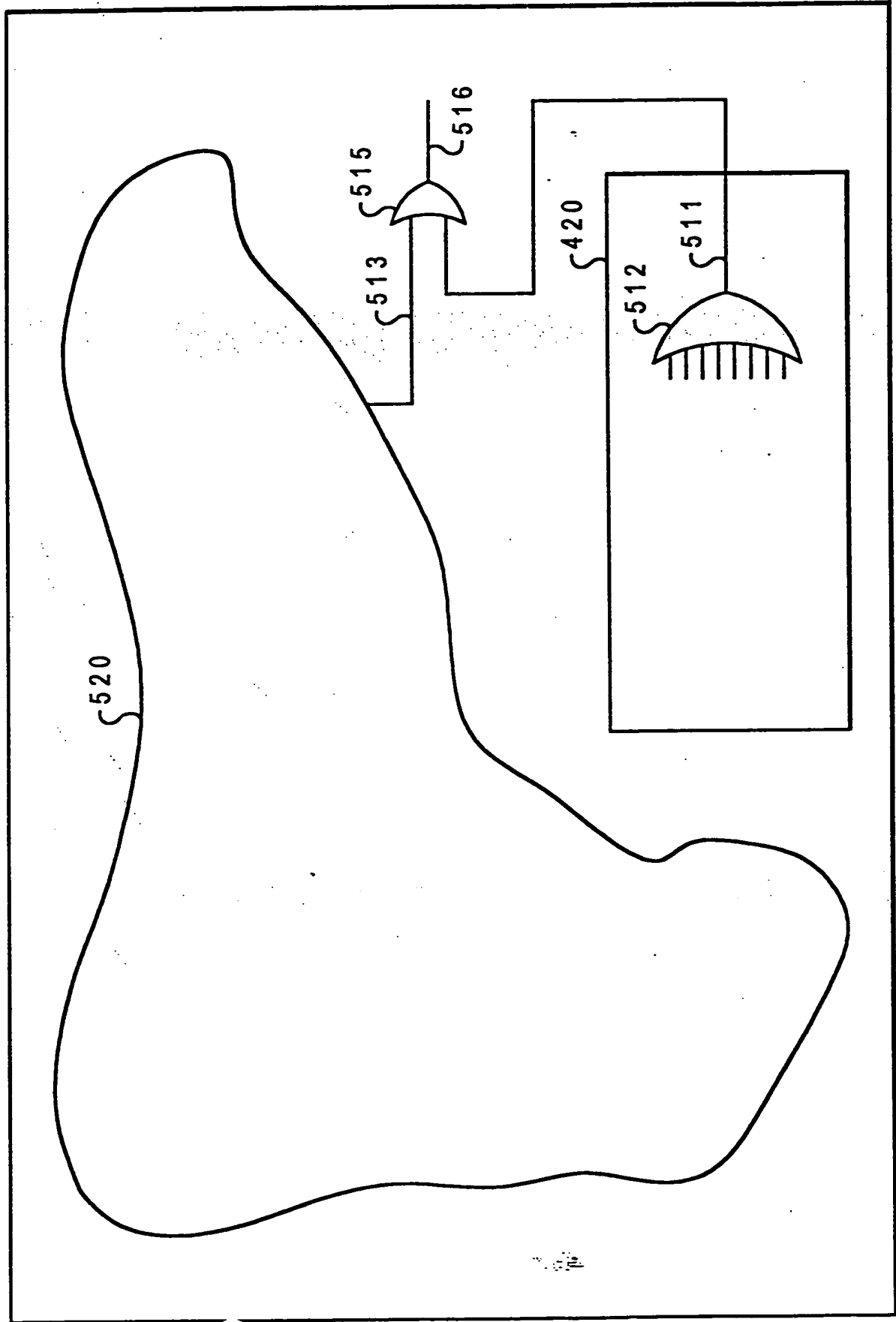


Fig. 5B

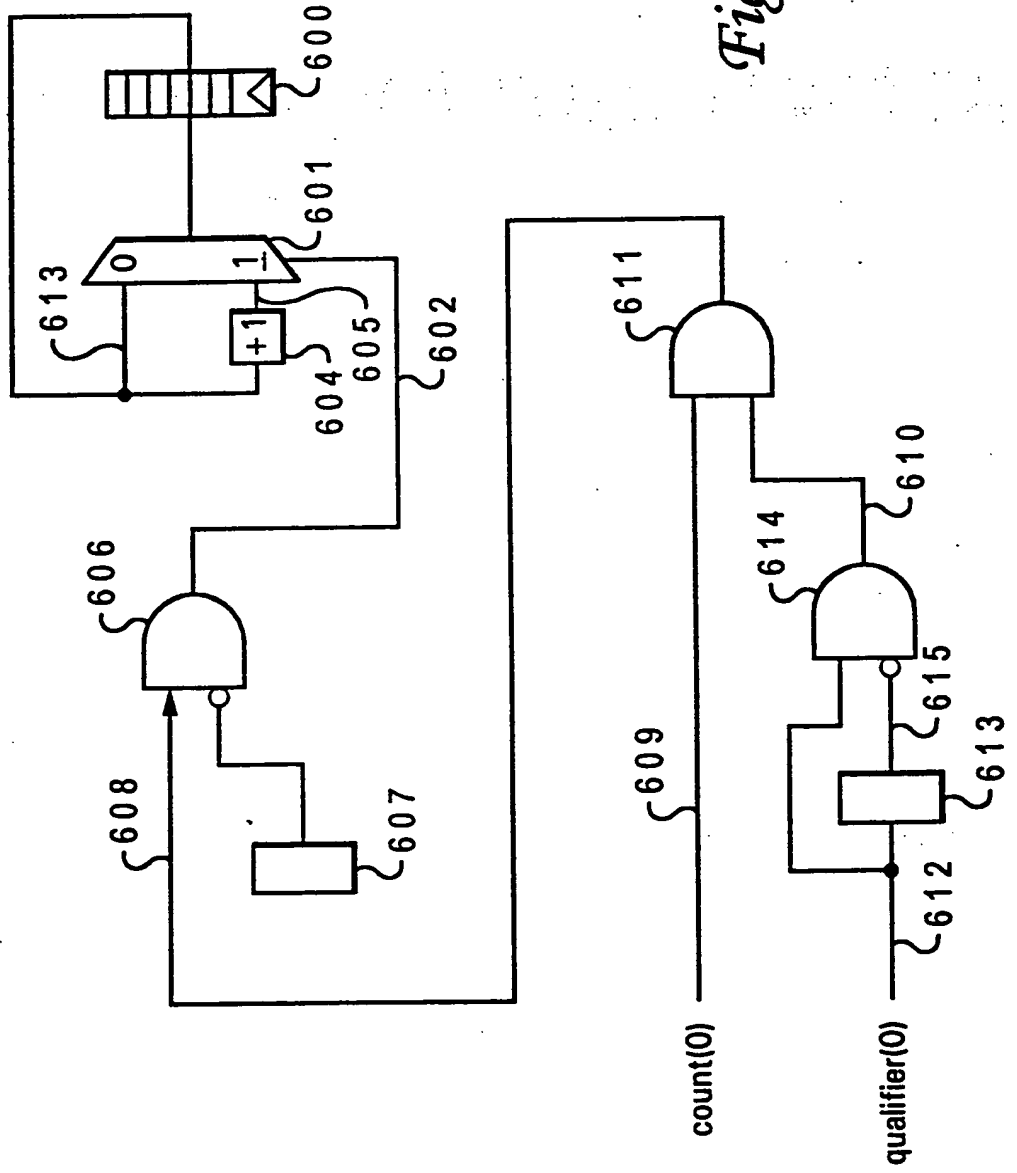


Fig. 6A





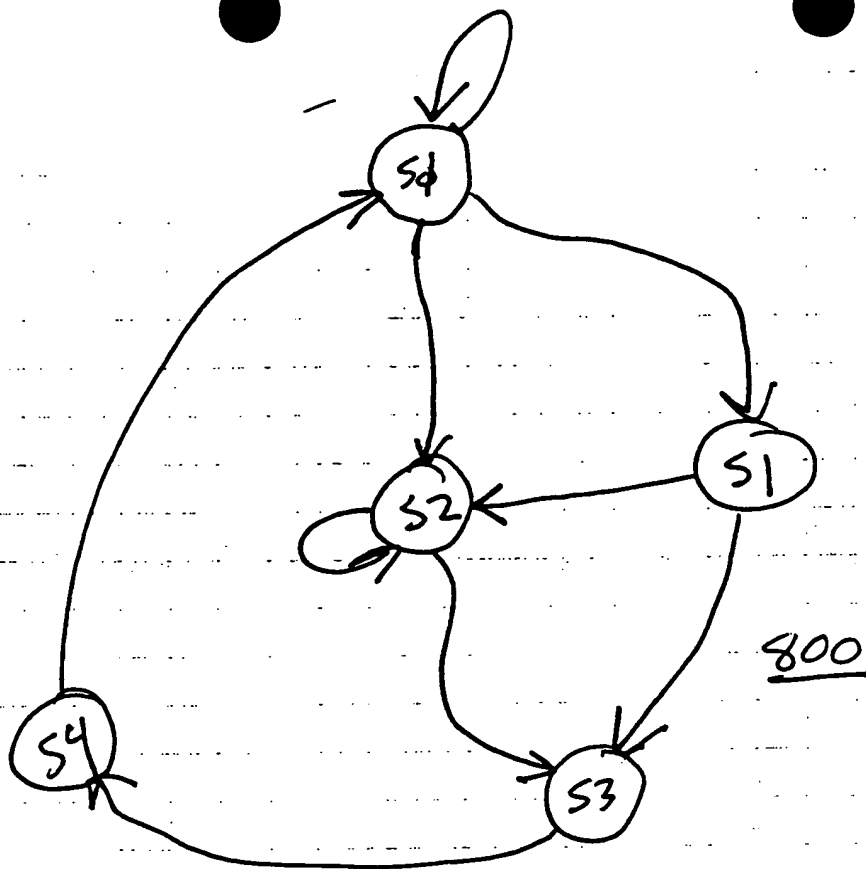


FIG. 8

(Prior Amt)

entity Fsm: Fsm

850

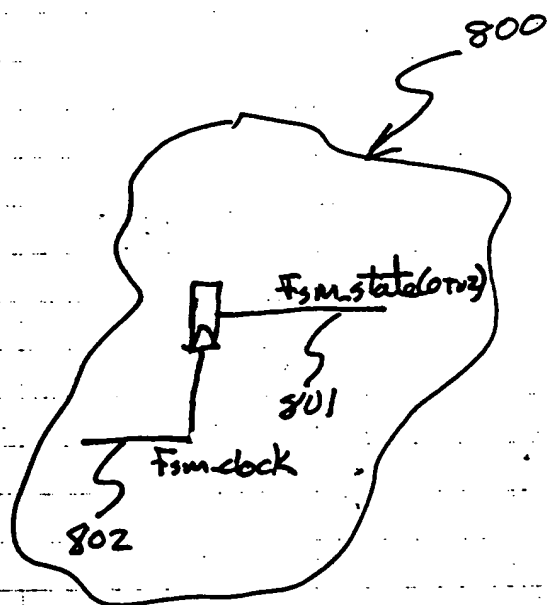


FIG. 8A  
(Prior Art)

entity Fsm IS

PORT (

.... ports for entity Fsm ....

);

ARCHITECTURE Fsm of Fsm IS

BEGIN

.... HDL code for Fsm and rest of the entity. ...

fsm-state(0 to 2) <= ... signal 801 ....

```
853 E --!! Embedded Fsm : exampleFsm;
859 E --!! clock          : (fsm_clock);
854 E --!! state_vector   : (fsm_state(0 to 2));
855 E --!! states         : (s0, s1, s2, s3, s4);
856 E --!! state_encoding  : ('000', '001', '010', '011', '100');
857 E --!! arcs           : (s0 => s0, s0 => s1, s0 => s2,
                           s1 => s2, s1 => s3, s2 => s2,
                           s2 => s3, s3 => s4, s4 => s0);
858 E --!! end Fsm;
```

852

86

END;

FIG. 8B

entity FSM:FSM

850

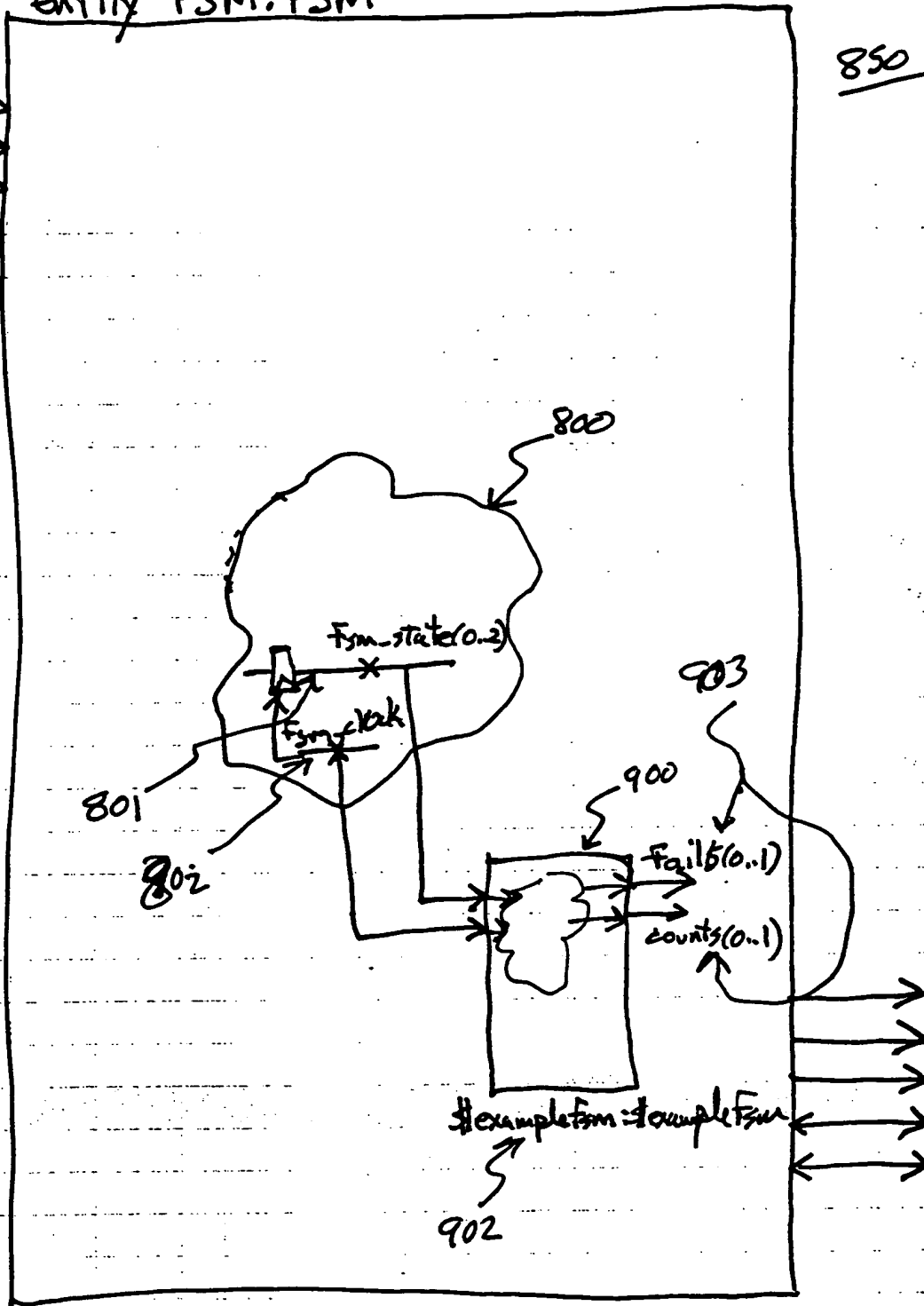


FIG. 9

TOP, TOP

1010a

X:Y



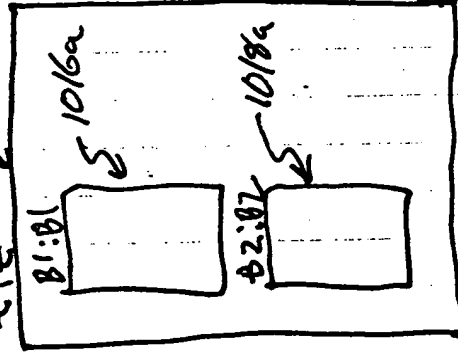
B3:03



1012a

1014a

Z:Z



B1:01

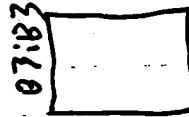
1016a

B2:02

1018a

1010b

X:Y



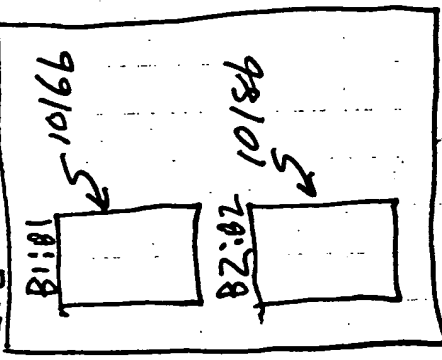
B3:03



1012b

1014b

Z:Z



B1:01

1016b

B2:02

1018b

1020

Y:Y

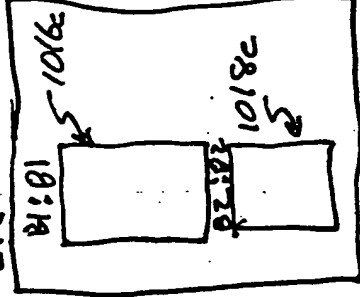


B4:04



1022

Z:Z



B1:01

1016c

B2:02

1018c

FIG. 10A

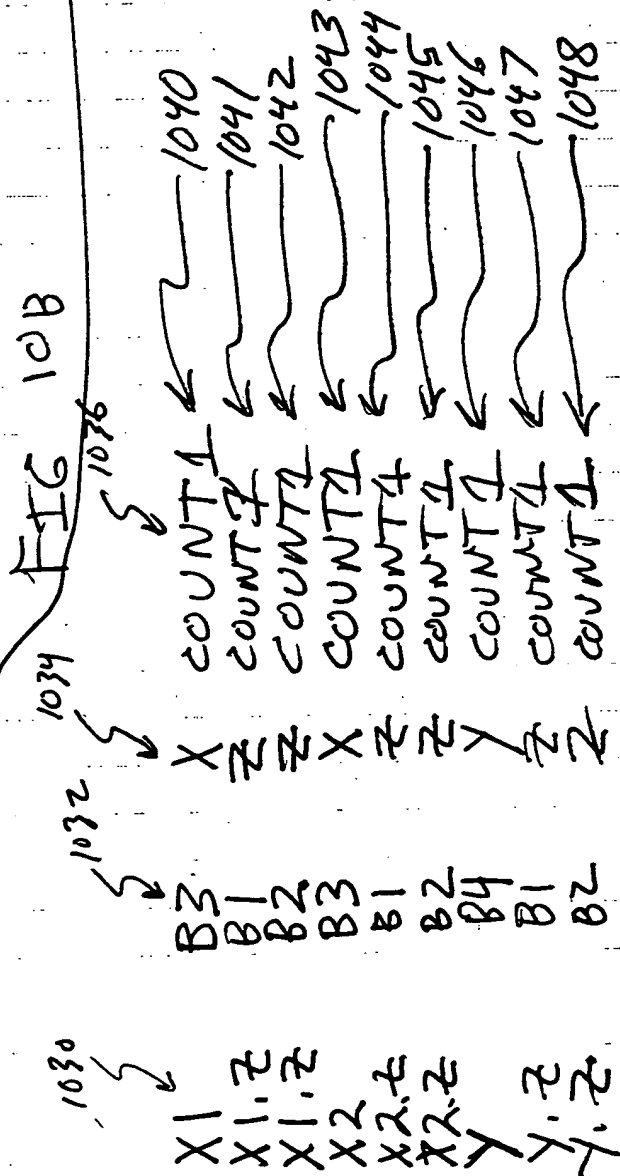
10303

10323

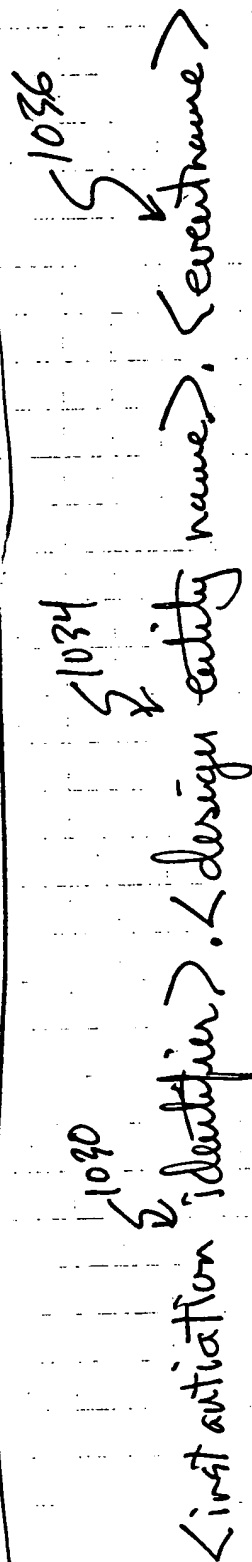
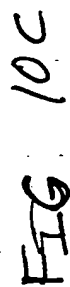
10343

10363

$\langle \text{instantiation identifier} \rangle, \langle \text{instrumentation entity name} \rangle, \langle \text{design entity name} \rangle, \langle \text{event name} \rangle$



103



10D 116

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